

TRANSITIONING Si4432 FROM REV V2 TO REV B

1. Purpose and Overview

The purpose of this document is to describe the changes between Revisions V2 and B to assist in the transition to the new revision. Pinout, TX/RX matching, register modifications, and overall performance improvements are discussed in this document.

The Si4432 Revision B addresses the errata items associated with revision V2 and offers additional performance enhancements. All errata items for Revision V2 are solved with the exception of some sensitivity desense on frequencies that are multiples of 30 MHz and a required register modification for data rates higher than 100 kbps. Both of these items are covered in the Revision B data sheet. Changes to the Si4432 Revision B are as follows:

- Improved output power to +20 dBm
- Improved sensitivity by 1 dB
- Improved OOK modem performance
- Improved OOK and FSK co-channel interferer performance
- Reduced current consumption
- Modified AFC settings and improved performance
- Improved TX data rate accuracy
- Modified and improved invalid preamble detection
- Improved synthesizer spurious performance

2. Pinout Changes

The pinout changes from V2 to B are minor and do not require a PCB board modification to transition to the new revision. Figure 1 illustrates the changed pins highlighted in red. Pin 5 previously required an external 1 μ F decoupling capacitor. This capacitor has been integrated, and the pin is not bonded to the device; so, connecting to Pin 5 will have no effect. Pin 6 is added to provide a control signal for a TX/RX switch to conserve the GPIO for other uses. Ant1 is a hardwired digital output equivalent to GPIO setting 10111, Antenna 1 Switch.

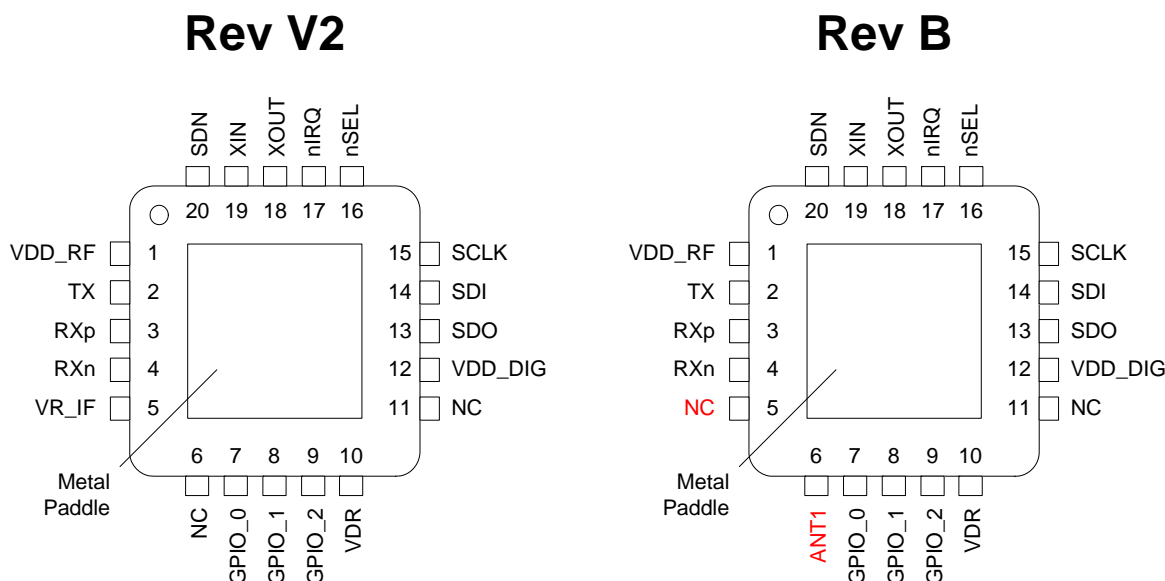


Figure 1. Pinout Changes

3. TX and RX Matching Components

The same matching structure and component values may be used for the Revision B receive match.

The same transmit match structure recommended in the Si4432 Revision 0.4 data sheet may still be used, but a change in component values is required. The V2 match structure included a resistor above Lchoke and a capacitor to ground at the TX pin. These components are no longer necessary but do not require a board change. The Si4432-B match structure is shown in Figure 2. For a complete PA matching discussion, see “AN435: Si4032/4432 PA Matching.”

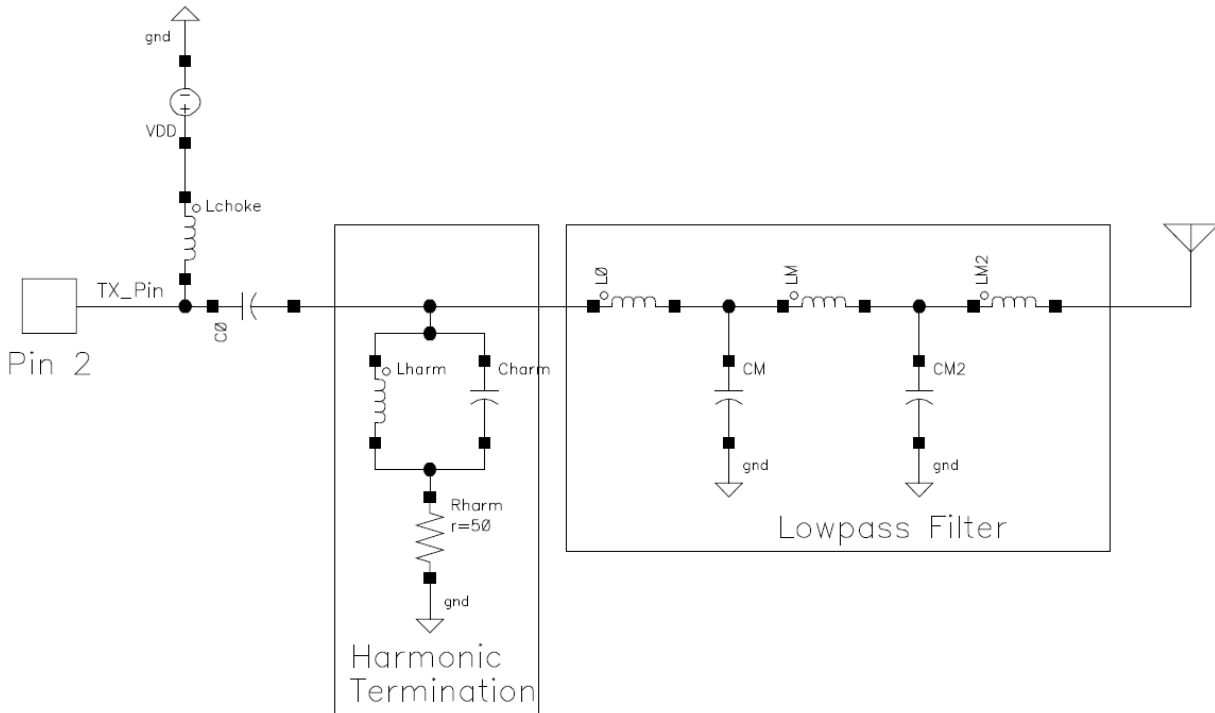


Figure 2. TX Match

Some early reference designs did not include the harmonic termination components. If the match structure being used is not equivalent to what is shown above or in Revision 0.4 of the Si4432 data sheet, contact technical support for advice on a transitional match using your existing structure.

The 4432-T-B1-C-xxx (formerly known as Si4432-DKDB2) single antenna with switch reference design for Revision B utilizes a different structure with a portion of the TX low-pass filter after the switch. This architecture results in better harmonic suppression due to harmonic regeneration caused by the switch. If current V2 performance is satisfactory with no low-pass filter after the switch, then Rev B will be able to achieve equivalent results.

4. Register Changes

The Revision V2 errata specified that register value changes were required for registers 59h, 5Ah, 66h, 65, and 6A. In Revision B, the default values of these registers have been changed and should no longer be altered.

The TX power register changed from two to three bits to enable more gain steps in the PA. If this setting is not changed then the output power will appear low. In revision V2 max power is set as txpow[1:0] = 11, and with Revision B max power is set as txpow[2:0] = 111.

All RX modem settings should be configured per the register calculator specific to Revision B, Si443x Register Settings_Rev B1-Vx.xls. The latest calculator may be downloaded from the Silicon Labs website: www.silabs.com. Table 1 highlights the modified registers. The calculator provides proper settings for all new or modified registers.

Table 1. Modified Registers from V2 to B

Add	R/W	Function/ Description	Data								POR Default
09	R/W	Crystal Oscillator Load Capacitance	xtalshft	xlcl[6]	xlcl[5]	xlcl[4]	xlcl[3]	xlcl[2]	xlcl[1]	xlcl[0]	7Fh
1D	R/W	AFC Loop Gearshift Override	afcbd	enafc	afcgearh[2]	afcgearh[1]	afcgearh[0]	1p5bypass	matap	ph0size	44h
1E	R/W	AFC Timing Control	swant_ timer[1]	swant_ timer[0]	shwait[2]	shwait[1]	shwait[0]	anwait[2]	anwait[1]	anwait[0]	0Ah
21	R/W	Clock Recovery Offset 2	rxosr [10]	rxosr[9]	rxosr[8]	stallctrl	ncoff[19]	ncoff[18]	ncoff[17]	ncoff[16]	01h
24	R/W	Clock Recovery Timing Loop Gain 1				rxncocomp	cgainx2	crgain[10]	crgain[9]	crgain[8]	02h
2A	R/W	AFC Limiter	Afclim[7]	Afclim[6]	Afclim[5]	Afclim[4]	Afclim[3]	Afclim[2]	Afclim[1]	Afclim[0]	00h
2B	R	AFC Correction Read	afc_corr[9]	afc_corr[8]	afc_corr[7]	afc_corr [6]	afc_corr[5]	afc_corr[4]	afc_corr[3]	afc_corr[2]	00h
2C	R/W	OOK Counter Value 1	afc_corr[1]	afc_corr[0]	ookfrzen	peakdeten	madeten	ookcnt[10]	ookcnt[9]	ookcnt[8]	18h
2D	R/W	OOK Counter Value 2	ookcnt[7]	ookcnt[6]	ookcnt[5]	ookcnt[4]	ookcnt[3]	ookcnt[2]	ookcnt[1]	ookcnt[0]	BCh
2E	R/W	Slicer Peak Hold	reserv.	attack[2]	attack[1]	attack[0]	decay[3]	decay[2]	decay[1]	decay[0]	26h
30	R/W	Data Access Control	enpacrx	lsbfrst	crcdonly	skip2ph	enpactx	encrc	crc[1]	crc[0]	8Dh
33	R/W	Header Control 2	skipsync	hdlen[2]	hdlen[1]	hdlen[0]	fixpklen	synlen[1]	synclen[0]	prelen[8]	22h
60	R/W	Channel Filter Coefficient Address	Inv_pre_th [3]	Inv_pre_th [2]	Inv_pre_th[1]	Inv_pre_th[0]	chfiladd[3]	chfiladd[2]	chfiladd[1]	chfiladd[0]	A0h
69	R/W	AGC Override 1	Reserved	SGL	aggcen	lnagain	pga[3]	pga[2]	pga[1]	pga[0]	20h
6D	R/W	TX Power	papeakval	papeaken	papeaklvl[1]	papeaklvl[0]	lna_sw	txpow[2]	txpow[1]	txpow[0]	18h
70	R/W	Modulation Mode Control 1			txdtrtscale	enphpwdn	manppol	enmaninv	enmanch	enwhite	0Ch

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