



July 1997  
Revised December 1999

## FST16292

### 12-Bit to 24-Bit Multiplexer/Demultiplexer Bus Switch

#### General Description

The Fairchild Switch FST16292 provides twelve 2:1 high-speed CMOS TTL-compatible multiplexer/demultiplexer bus switches. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The select pin connects the A Port to the selected B Port output. The A<sub>2</sub> Ports are not externally connected, thus have a 500Ω pull-down resistor to ground.

#### Features

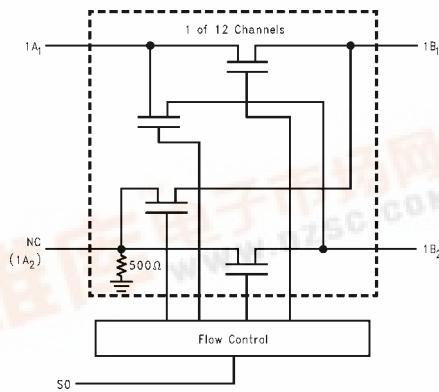
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I<sub>CC</sub>.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.
- Internal 500Ω pull-down resistor on A<sub>2</sub> port.

#### Ordering Code:

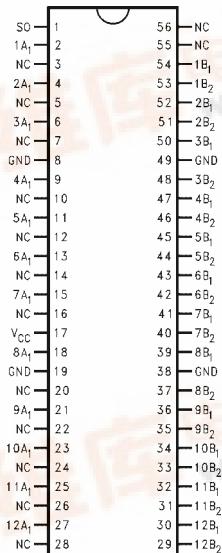
Order Number	Package Number	Package Description
FST16292MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
FST16292MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Logic Diagram



#### Connection Diagram



#### Pin Descriptions

Pin Name	Description
SO	Data-select input
A <sub>1</sub>	Bus A
B <sub>1</sub> , B <sub>2</sub>	Bus B

#### Truth Table

SO	A <sub>1</sub>	A <sub>2</sub>	Function
L	B <sub>1</sub>	B <sub>2</sub>	A <sub>1</sub> = B <sub>1</sub> , A <sub>2</sub> = B <sub>2</sub>
H	B <sub>2</sub>	B <sub>1</sub>	A <sub>1</sub> = B <sub>2</sub> , A <sub>2</sub> = B <sub>1</sub>

## FST16292 12-Bit to 24-Bit Multiplexer/Demultiplexer Bus Switch

**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Switch Voltage ( $V_S$ )	-0.5V to +7.0V
DC Input Voltage ( $V_{IN}$ ) (Note 2)	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ ) $V_{IN} < 0V$	-50mA
DC Output ( $I_{OUT}$ ) Sink Current	128mA
DC $V_{CC}/GND$ Current ( $I_{CC}/I_{GND}$ )	+/- 100mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150 °C

**Recommended Operating Conditions**

Power Supply Operating ( $V_{CC}$ )	4.0V to 5.5V
Input Voltage ( $V_{IN}$ )	0V to 5.5V
Output Voltage ( $V_{OUT}$ )	0V to 5.5V
Input Rise and Fall Time ( $t_r, t_f$ )	
Switch Control Input	0ns/V to 5ns/V
Switch I/O	0ns/V to DC
Free Air Operating Temperature ( $T_A$ )	-40 °C to +85 °C

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40$ °C to +85 °C			Units	Conditions
			Min	Typ (Note 3)	Max		
$V_{IK}$	Clamp Diode Voltage	4.5			-1.2	V	$I_{IN} = -18mA$
$V_{IH}$	HIGH Level Input Voltage	4.0-5.5	2.0			V	
$V_{IL}$	LOW Level Input Voltage	4.0-5.5			0.8	V	
$I_I$	Input Leakage Current	5.5			$\pm 1.0$	$\mu A$	$0 \leq V_{IN} \leq 5.5V$
		0			10	$\mu A$	$V_{IN} = 5.5V$
$I_{OZ}$	OFF-STATE Leakage Current	5.5			$\pm 1.0$	$\mu A$	$0 \leq A, B \leq V_{CC}$
$R_{ON}$	Switch On Resistance (Note 4)	4.5		4	7	$\Omega$	$V_{IN} = 0V, I_{IN} = 64mA$
		4.5		4	7	$\Omega$	$V_{IN} = 0V, I_{IN} = 30mA$
		4.5		8	12	$\Omega$	$V_{IN} = 2.4V, I_{IN} = 15mA$
		4.0		14	20	$\Omega$	$V_{IN} = 2.4V, I_{IN} = 15mA$
$I_{CC}$	Quiescent Supply Current	5.5			3	$\mu A$	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	5.5			2.5	mA	One input at 3.4V Other inputs at $V_{CC}$ or GND

**Note 3:** Typical values are at  $V_{CC} = 5.0V$  and  $T_A = +25^\circ C$

**Note 4:** Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

## AC Electrical Characteristics

Symbol	Parameter	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ , $C_L = 50\text{pF}$ , $R_U = RD = 500\Omega$				Units	Conditions	Figure No.			
		$V_{CC} = 4.5 - 5.5\text{V}$		$V_{CC} = 4.0\text{V}$							
		Min	Max	Min	Max						
$t_{PHL}, t_{tPLH}$	Prop Delay Bus to Bus (Note 5)		0.25		0.25	ns	$V_I = \text{OPEN}$	Figure 1 Figure 2			
$t_{PHL}, t_{tPLH}$	Prop Delay S0 to A <sub>1</sub>	1.5	7.0		7.4	ns	$V_I = \text{OPEN}$	Figure 1 Figure 2			
$t_{PZL}, t_{tPZH}$	Output Enable Time S0 to B <sub>1</sub> or B <sub>2</sub>	1.0	6.7		7.0	ns	$V_I = 7\text{V}$ for $t_{PZL}$ $V_I = \text{OPEN}$ for $t_{tPZH}$	Figure 1 Figure 2			
$t_{PLZ}, t_{tPHZ}$	Output Disable Time S0 to B <sub>1</sub> or B <sub>2</sub>	1.0	7.5		7.8	ns	$V_I = 7\text{V}$ for $t_{PLZ}$ $V_I = \text{OPEN}$ for $t_{tPHZ}$	Figure 1 Figure 2			

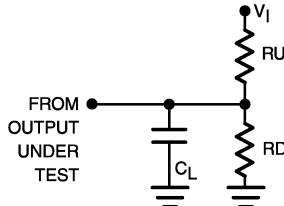
**Note 5:** This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

## Capacitance (Note 6)

Symbol	Parameter	Typ	Max	Units	Conditions
$C_{IN}$	Control pin Input Capacitance	3		pF	$V_{CC} = 5.0V$
$C_{I/O}$	Input/Output Capacitance	10		pF	$V_{CC} = 5.0V, S0 = GND$

**Note 6:**  $T_A = +25^\circ\text{C}$ ,  $f = 1 \text{ MHz}$ , Capacitance is characterized but not tested.

## AC Loading and Waveforms



Note: Input driven by  $50 \Omega$  source terminated in  $50 \Omega$

Note:  $C_L$  includes load and stray capacitance

Note: Input PRR = 1.0 MHz,  $t_w = 500$  ns

FIGURE 1. AC Test Circuit

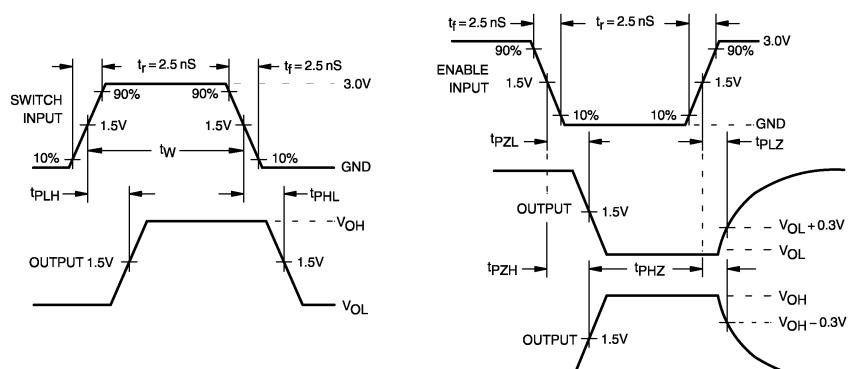
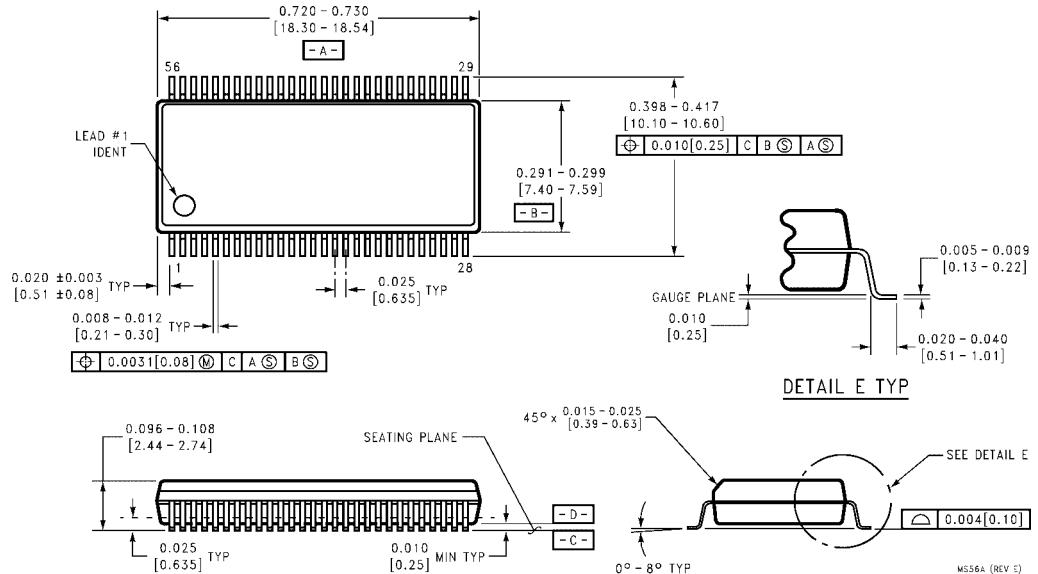
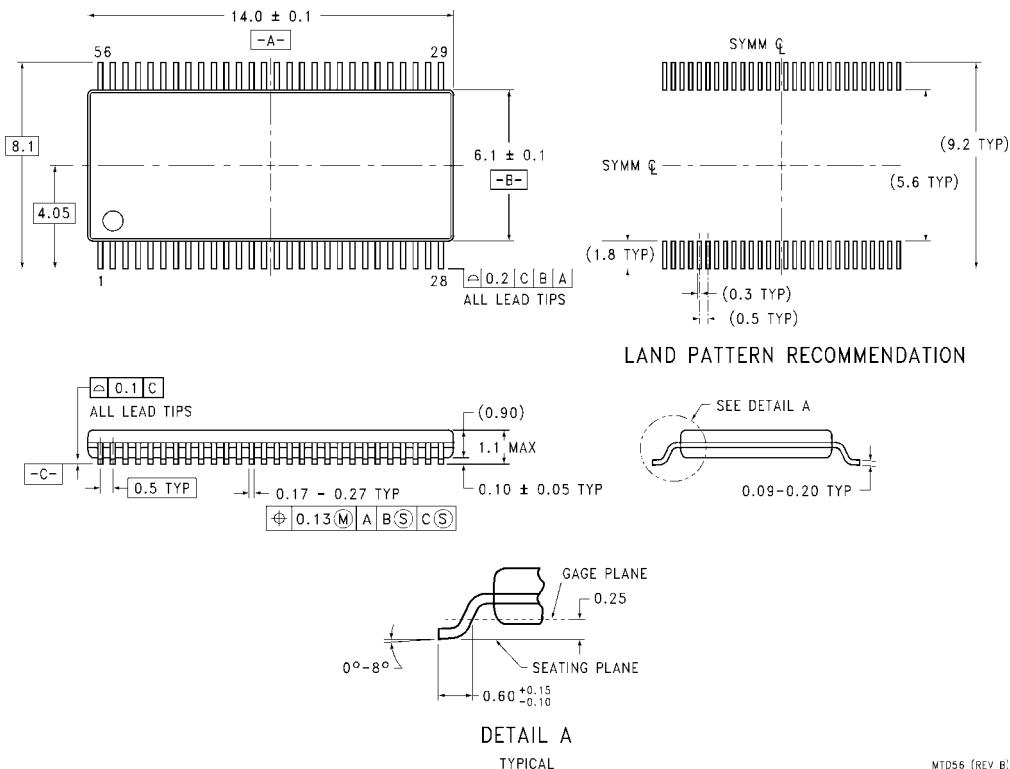


FIGURE 2. AC Waveforms

**Physical Dimensions** inches (millimeters) unless otherwise noted

56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide  
Package Number MS56A

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide  
Package Number MTD56

**Technology Description**

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

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